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705

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10077967	02/20/2002	~~257~~ 438	107	2822	TRINH

**APPLICANTS: Kim Sarah; List R.; Kellar Scot;

**CONTINUING DATA VERIFIED: MT none)

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** FOREIGN APPLICATIONS VERIFIED: MT none

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☒ no	ATTORNEY DOCKET NO	
35 USC 119 conditions met	☐ yes ☒ no	219.40232X00	
Verified and Acknowledged Examiners's intials	M. T.		

TITLE : Process of vertically stacking multiple wafers supporting different active integrated circuit (IC) devices

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER	Primary Examiner	Applicati n Examiner	
	PREPARED FOR ISSUE		

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